SMBus/I²C Fan Speed Controller in SOT-23

FEATURES

- **Complete SMBus/I²C™ Brushless DC Fan Speed Control System in a 5-Pin SOT-23 package**
- 0.75Ω PMOS Linear Regulator with 180mA Output Current Rating
- 0V to 4.922V Output Voltage Range Controlled by a 6-Bit DAC
- Simple 2-Wire SMBus/I²C Interface
- 250ms Internal Timer Ensures Fan Start-Up
- Current Limit and Thermal Shutdown
- Fault Status Indication via SMBus Host Readback

APPLICATIONS

- Notebook Computers
- Spot Cooling
- Portable Instruments
- Battery-Powered Systems
- DC Motor Control
- White LED Power Supplies
- Programmable Low Dropout Regulator

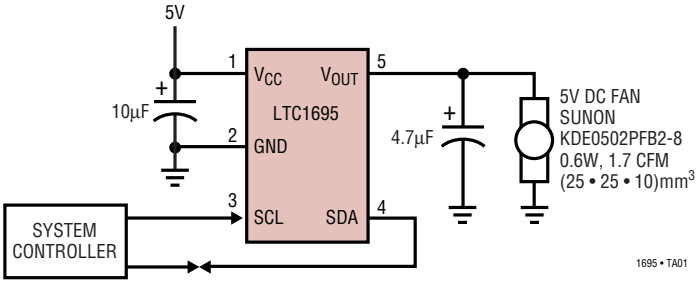
DESCRIPTION

The LTC®1695 fan speed controller provides all the functions necessary for a power management microprocessor to regulate the speed of a 5V brushless DC fan via a 2-wire SMBus/I²C interface. Fan speed is controlled according to the system's required temperature profile and permits lower fan power consumption, longer battery run time and lower acoustical generated noise versus systems that only provide simple on-off control for the fan.

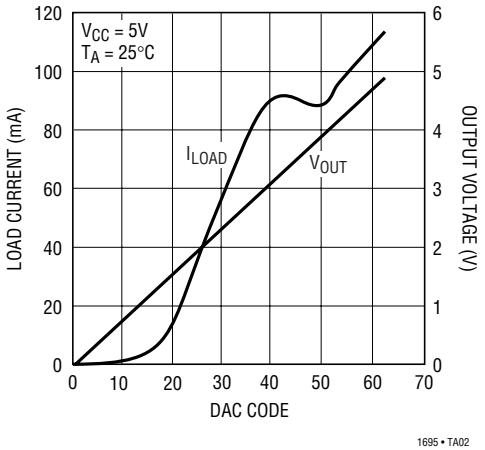
The LTC1695 incorporates a 180mA low dropout linear regulator, a 2-wire SMBus/I²C interface and a 6-bit DAC. Fan speed is controlled by varying the fan's terminal voltage through the output voltage of the LTC1695's linear regulator. The LTC1695's output voltage is programmed by sending a 6-bit digital code to the LTC1695 DAC via the SMBus. To eliminate fan start-up problems at lower fan voltages, users can enable the LTC1695's boost start feature that provides the DAC's full-scale output voltage for 250ms before decreasing to the programmed output voltage.

The LTC1695 includes output current limiting and thermal shutdown as well as status monitors that can be read back by the microprocessor during fault conditions. The LTC1695 is available in a 5-lead SOT-23 package.

TYPICAL APPLICATION



Fan Voltage and Current vs DAC Code



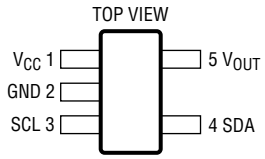
ABSOLUTE MAXIMUM RATINGS

(Note 1)

Terminal Voltages
- Supply Voltage (V_{CC}) 7V
- All Other Inputs ..... –0.3V to (V_{CC} + 0.3V)

Operating Temperature Range ..... 0°C to 70°C
Junction Temperature ..... 125°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION



S5 PACKAGE
5-LEAD PLASTIC SOT-23

T_{JMAX} = 125°C, θ_{JA} = 256°C/W

SEE THE APPLICATIONS INFORMATION SECTION.

ORDER PART NUMBER
LTC1695CS5
S5 PART MARKING
LTIY

Consult factory for Industrial and Military grade parts.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = 5V unless otherwise stated.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{CC}	Supply Voltage Range			4.5	5	5.5	V
I_{CC}	Supply Current, Operating Supply Current, Shutdown	V_{OUT} = Full Scale, I_{LOAD} = 150mA DAC Code = 0	● ●		150.7 80	155 200	mA µA
DAC							
	DAC Resolution	Guaranteed Monotonic	●		6		Bits
V_{LSB}	1LSB Resolution	I_{LOAD} = 1mA	●	73	78	83	mV
V_{OS}	Offset Error	I_{LOAD} = 1mA	●			±1	LSB
DNL	Differential Nonlinearity	I_{LOAD} = 1mA (Note 2)	●			±0.75	LSB
INL	Integral Nonlinearity	I_{LOAD} = 1mA (Note 2)	●			±0.75	LSB
V_{FS}	V_{OUT}, DAC Full Scale	I_{LOAD} = 20mA I_{LOAD} = 150mA	● ●	4.5 4.5	4.93 4.9		V V
V_{ZS}	V_{OUT}, DAC Zero Scale	R_{LOAD} = 1kΩ	●		0	85	mV
$R_{ON(P)}$	P-Channel On Resistance	I_{LOAD} = 150mA			0.75		Ω
Timer and Thermal Shutdown							
V_{UVLO}	Undervoltage Lockout Voltage	Rising V_{CC}	●	2.3	2.9	3.5	V
T_{BST_ST}	Boost Start Timer	I_{LOAD} = 10mA, C_{LOAD} = 4.7µF	●	75	250	1000	ms
$T_{THERMAL}$	Thermal Shutdown Temperature	(Note 3)			155		°C
I_{FAULT}	Output Current Limit Threshold	V_{OUT} = 0V, DAC Code = 63	●	180	390	850	mA
SMBus SCL, SDA Inputs							
V_{IH}	Input High Threshold		●	2.1			V
V_{IL}	Input Low Threshold		●			0.8	V
I_{IN}	Input Current	SCL, SDA = 0V or 5V	●		±0.1	±5	µA
C_{IN}	Input Capacitance	(Note 3)			3		pF
t_{ON}	Switch On Time from Stop Condition (f_{SMBus} = 100kHz)	V_{OUT} from Zero Scale to Full Scale, I_{LOAD} = 1mA, C_{LOAD} = 4.7µF	●		50	500	µs
t_{OFF}	Switch Off Time from Stop Condition (f_{SMBus} = 100kHz)	V_{OUT} from Full Scale to Zero Scale, I_{LOAD} = 150mA, C_{LOAD} = 4.7µF	●		150	500	µs
V_{OL}	SDA Output Low Voltage	I_{PULLUP} = 3mA	●		150	400	mV

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = 5V unless otherwise stated.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
SMBus TIMING (Note 4)							
f_{SMB}	SMBus Operating Frequency		●	10		100	kHz
t_{BUF}	Bus Free Time Between Stop and Start		●	4.7			µs
$t_{HD(STA)}$	Hold Time After (Repeated) Start Condition		●	4.0			µs
$t_{SU(STA)}$	Repeated Start Condition Setup Time		●	4.7			µs
$t_{SU(STO)}$	Stop Condition Setup Time		●	4.0			µs
$t_{HD(DAT)}$	Data Hold Time		●	300			ns
$t_{SU(DAT)}$	Data Setup Time		●	250			ns
t_{LOW}	Clock Low Period		●	4.7			µs
t_{HIGH}	Clock High Period		●	4.0		50	µs
t_f	Clock/Data Fall Time		●			300	ns
t_r	Clock/Data Rise Time		●			1000	ns

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

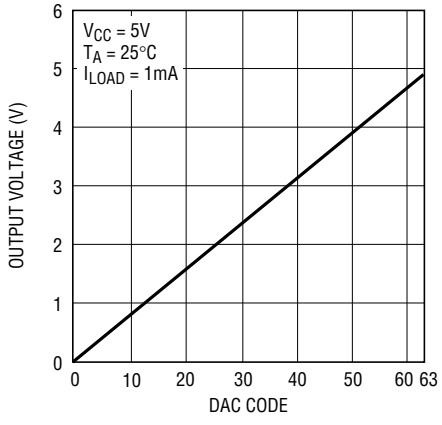
Note 2: INL, DNL specs are specified under a 1mA I_{LOAD} condition to keep the linear regulator from operating in dropout at higher DAC codes. DNL is measured from code 0 to code 63, taking into account the untrimmed offset at code 0. Please refer to the Definitions section for more details.

Note 3: This typical specification is based on lab measurements and is not production tested.

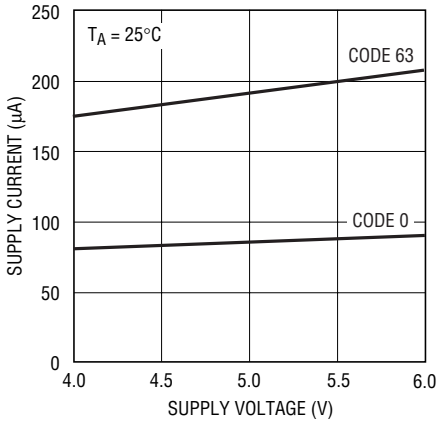
Note 4: Guaranteed by design and not tested. Please refer to the Timing Diagram section for additional information.

TYPICAL PERFORMANCE CHARACTERISTICS

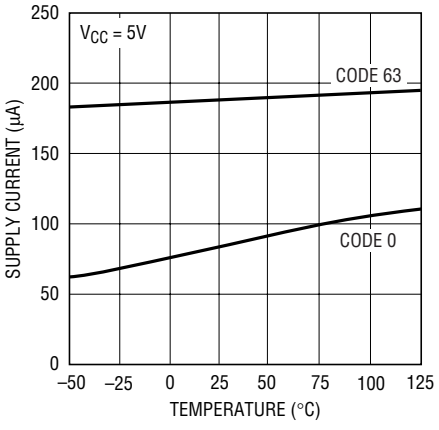
Output Voltage vs DAC Code



No Load Supply Current vs Supply Voltage

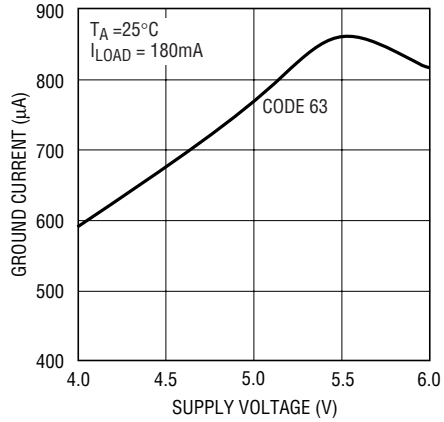


No Load Supply Current vs Temperature



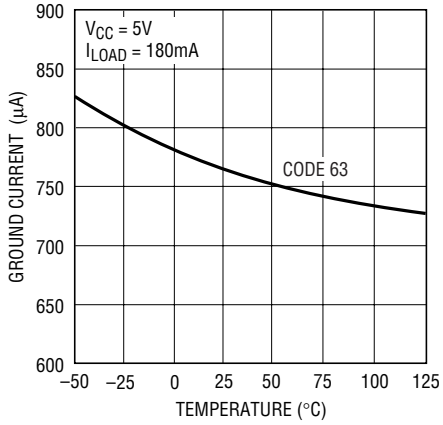
TYPICAL PERFORMANCE CHARACTERISTICS

Ground Current (Dropout Mode) vs Supply Voltage



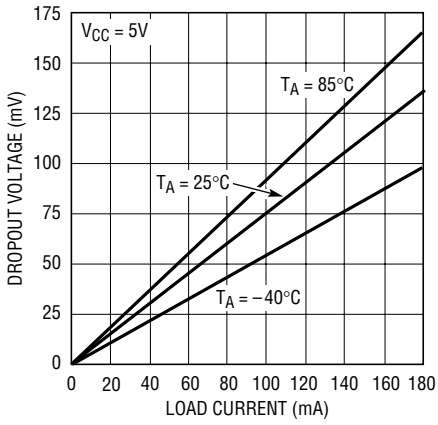
1695 • G04

Ground Current (Dropout Mode) vs Temperature



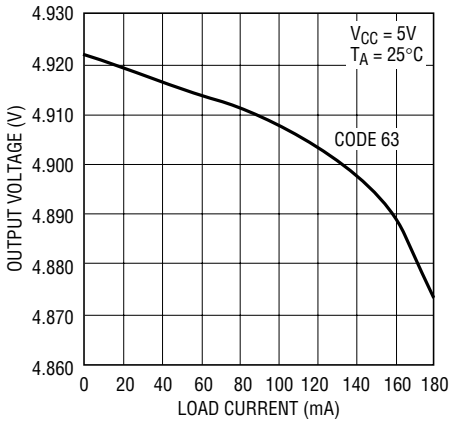
1695 • G05

Dropout Voltage vs Load Current



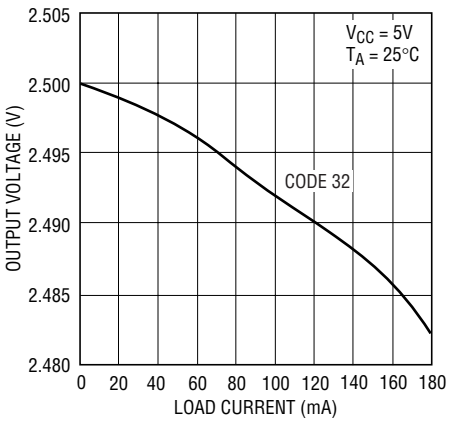
1695 • G06

Output Voltage (Full Scale) vs Load Current



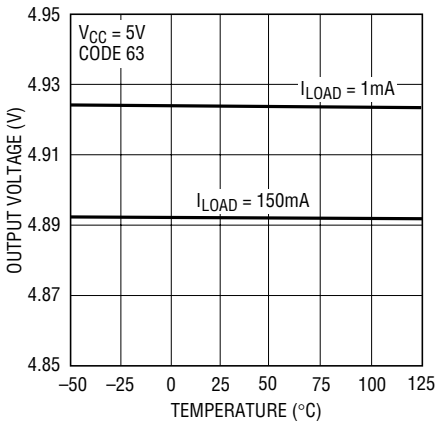
1695 • G07

Output Voltage (Midscale) vs Load Current



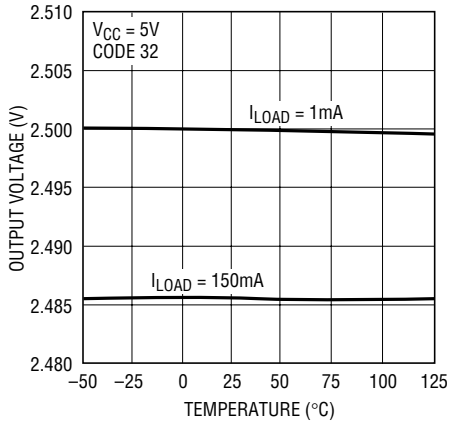
1695 • G08

Output Voltage (Full Scale) vs Temperature



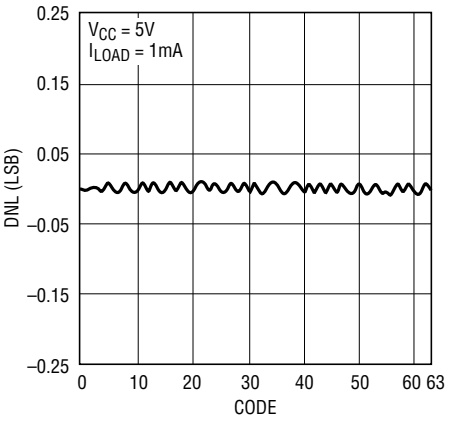
1695 • G09

Output Voltage (Midscale) vs Temperature



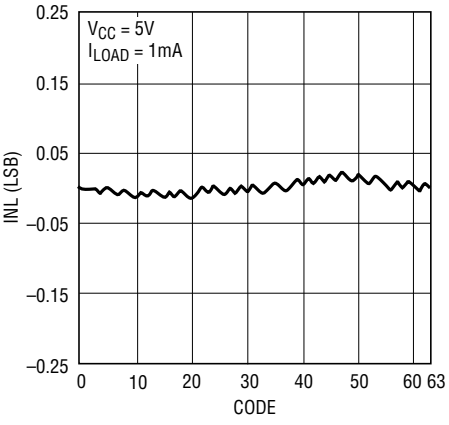
1695 • G10

Differential Nonlinearity (DNL)



1695 • G11

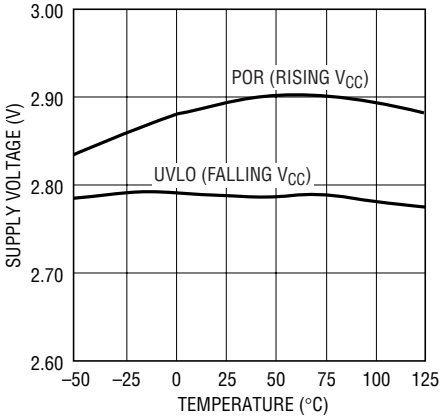
Integral Nonlinearity (INL)



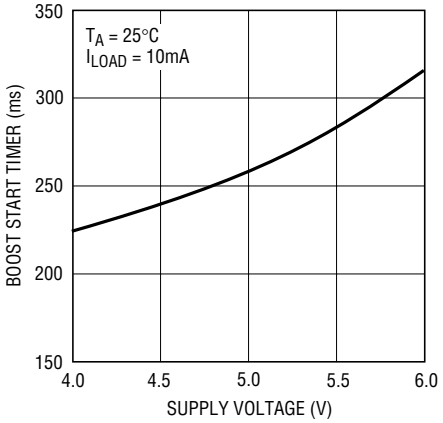
1695 • G12

TYPICAL PERFORMANCE CHARACTERISTICS

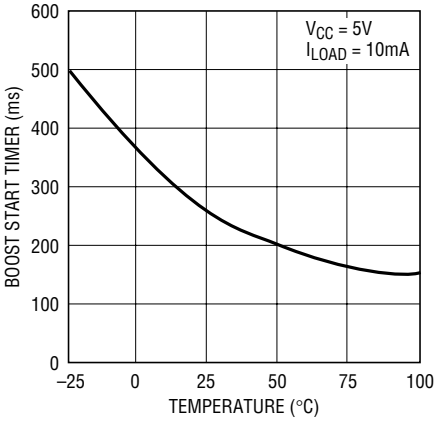
POR and UVLO vs Temperature



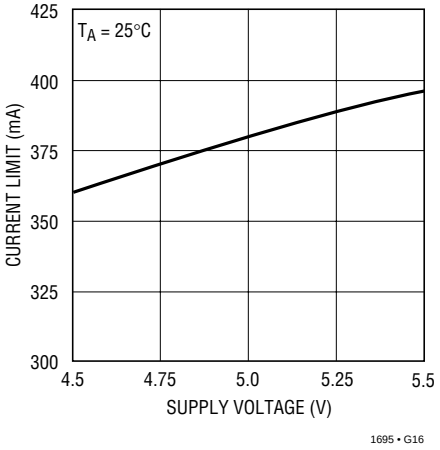
Boost Start Timer vs Supply Voltage



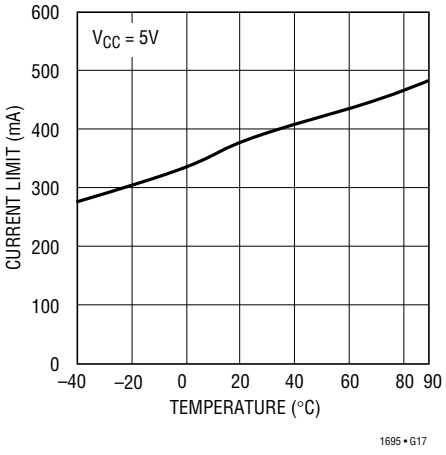
Boost Start Timer vs Temperature



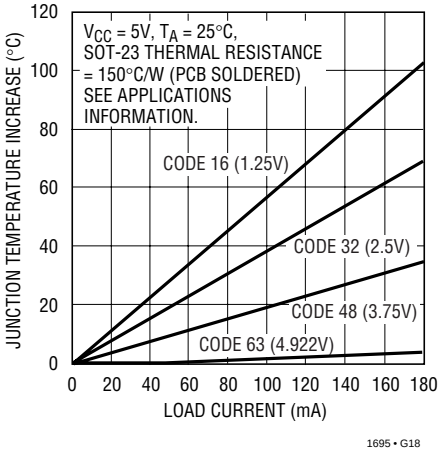
Current Limit Threshold vs Supply Voltage



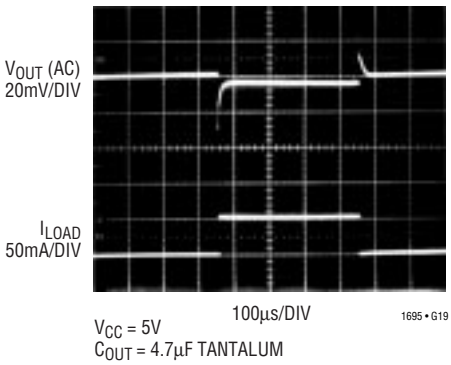
Current Limit Threshold vs Temperature



Junction Temperature Increase vs Load Current

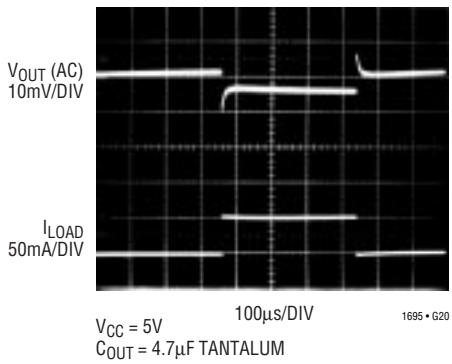


Load Transient Response Code 32, 5mA to 55mA



VCC = 5V
COUT = 4.7µF TANTALUM

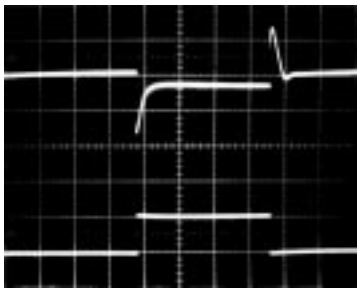
Load Transient Response Code 32, 50mA to 100mA



VCC = 5V
COUT = 4.7µF TANTALUM

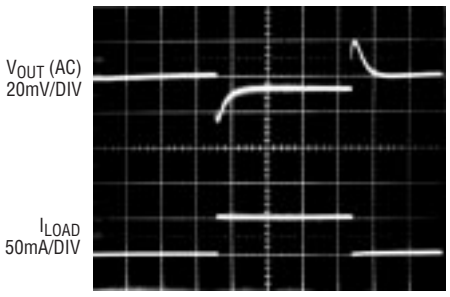
TYPICAL PERFORMANCE CHARACTERISTICS

Load Transient Response Dropout (Code 63), 5mA to 55mA



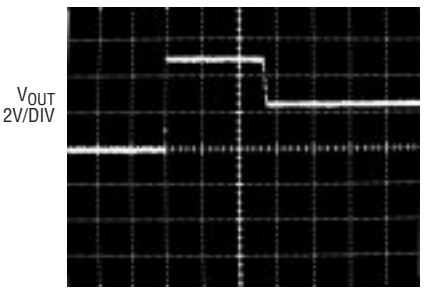
V_{CC} = 5V
C_{OUT} = 4.7µF TANTALUM

Load Transient Response Dropout (Code 63), 50mA to 100mA



V_{CC} = 5V
C_{OUT} = 4.7µF TANTALUM

Boost Start Timer



V_{CC} = 5V
C_{IN} = 10µF
C_{OUT} = 4.7µF
I_{LOAD} = 1mA

PIN FUNCTIONS

V_{CC} (Pin 1): Power Supply Input. V_{CC} supplies current to the internal control circuitry, serves as the reference for the 6-bit DAC and acts as the power path for the P-channel low dropout linear regulator. Bypass V_{CC} directly to ground with a low ESR capacitor ≥10µF.

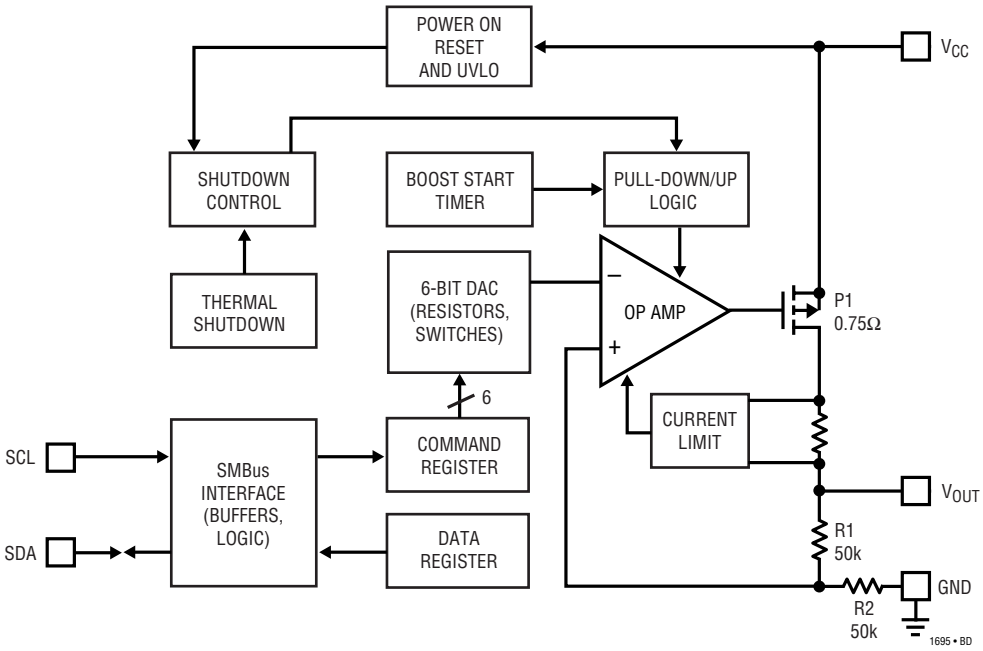
GND (Pin 2): Ground. Tie GND to the ground plane.

SCL (Pin 3): SMBus Clock Input. Data is shifted into SDA on the rising edge of the SCL clock signal during data transfer.

SDA (Pin 4): SMBus Bidirectional Data Input/Digital Output. SDA is an open drain output and requires a pull-up resistor or current source to V_{CC}. Data is shifted into SDA and acknowledged by SDA.

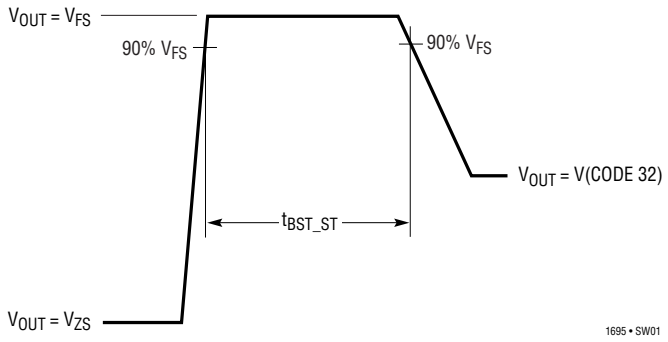
V_{OUT} (Pin 5): Linear Regulator Output. Connect directly to the fan's $+V_E$ terminal. V_{OUT} is set to V_{ZS} (code 0) on power-up. For good transient response and stability, use a general purpose, low cost, medium ESR (0.1Ω to 1Ω) tantalum or electrolytic capacitor. LTC recommends a surface mount tantalum capacitor of ≥4.7µF.

BLOCK DIAGRAM

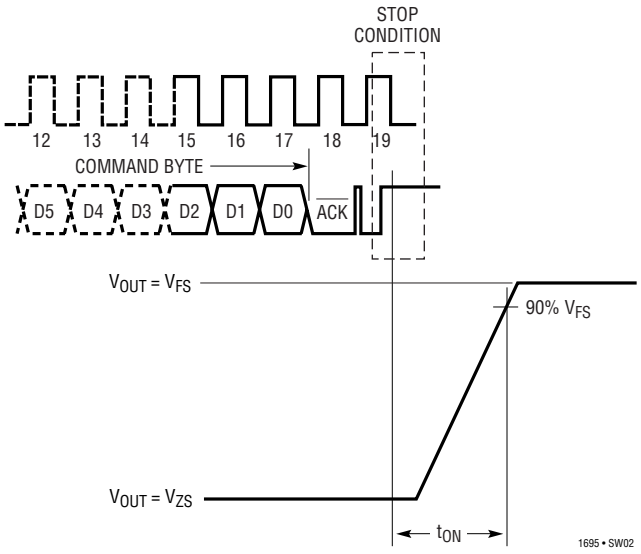


SWITCHING WAVEFORMS

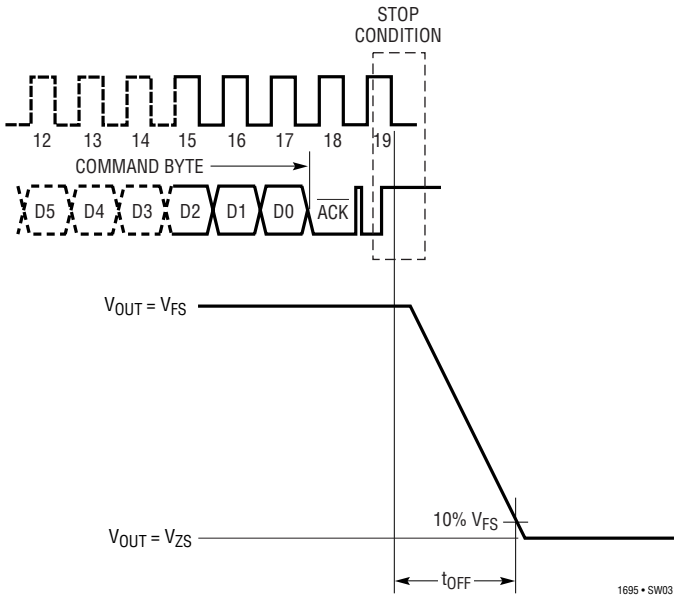
Boost Start Timer Measurement
I_{LOAD} = 10mA, C_{LOAD} = 4.7µF



Output Switch On Time Measurement
Code = 63, I_{LOAD} = 1mA, C_{LOAD} = 4.7µF
f_{SMBus} =100kHz

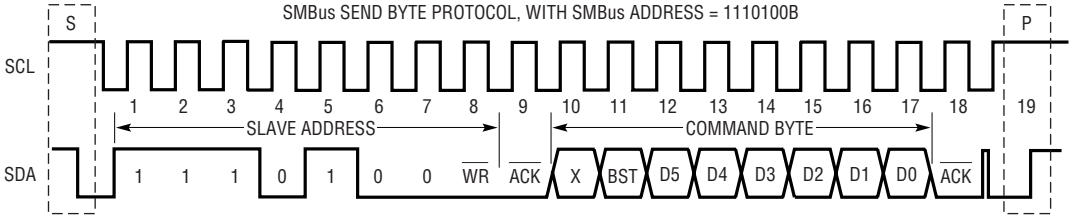


Output Switch Off Time Measurement
Code = 0, I_{LOAD} = 150mA, C_{LOAD} = 4.7µF
f_{SMBus} =100kHz

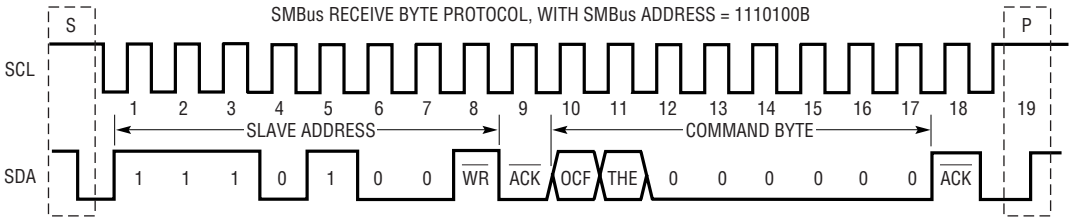


TIMING DIAGRAM

Operating Sequence



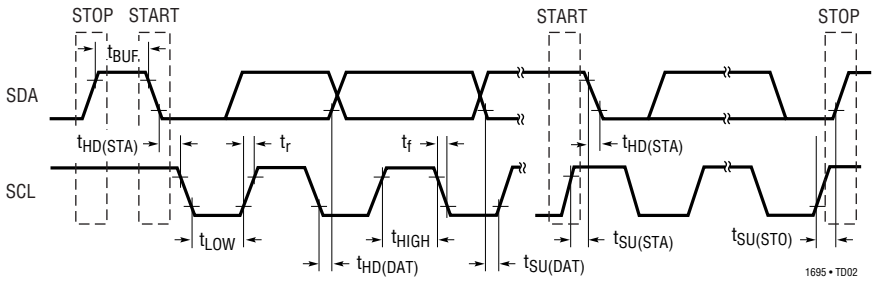
S = SMBus START BIT
P = SMBus STOP BIT
BST = 1 ENABLES THE BOOST START TIMER
D5 TO D0 = 6-BIT INPUT CODE FOR THE DAC (D5 = MSB)
X = DON'T CARE



S = SMBus START BIT
P = SMBus STOP BIT
OCF = 1 SIGNALS THAT THE LTC1695 IS IN CURRENT LIMIT
THE = 1 SIGNALS THAT THE LTC1695 IS IN THERMAL SHUTDOWN

1695 • TD01

Timing for SMBus Interface



1695 • TD02

DEFINITIONS

Resolution: The number of DAC output states (2^N) that divide the full-scale range. The resolution does not imply linearity.

Full-Scale Voltage (V_{FS}): The regulator output voltage (V_{OUT}) if all DAC bits are set to ones (code 63).

Voltage Offset Error (V_{OS}): The regulator output voltage if all DAC bits are set to zeros. The LDO amplifier can have a true negative offset, but due to the LTC1695's single supply operation, V_{OUT} cannot go below ground. If the offset is negative, V_{OUT} will remain near 0V resulting in the transfer curve shown in Figure 1.

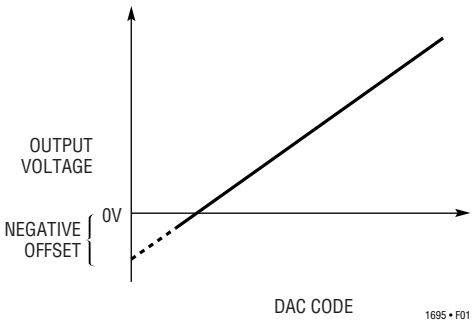


Figure 1. Effect of Negative Offset

The offset of the part is measured at the first code (code 1) that produces an output voltage 0.5LSB greater than the previous code.

$$V_{OS} = V_{OUT} - [(Code \bullet V_{FS})/(2^N - 1)]$$

Least Significant Bit (V_{LSB}): The least significant bit or the ideal voltage difference between two successive codes.

$$V_{LSB} = (V_{FS} - V_{OS})/(2^N - 1)$$

Table 1. Nominal V_{LSB} and V_{FS} values

V_{CC}	V_{LSB}	V_{FS}
4.5V	70.3mV	4.430V
5.0V	78.1mV	4.922V
5.5V	85.9mV	5.414V

INL: Integral nonlinearity is the maximum deviation from a straight line passing through the endpoints of the DAC transfer curve. Due to the LTC1695's single supply operation and the fact that V_{OUT} cannot go below ground, linearity is measured between full scale and the first code (code 01) that guarantees a positive output. The INL error at a given input code is calculated as follows:

$$INL = (V_{OUT} - V_{IDEAL}))/V_{LSB}$$

$$V_{IDEAL} = (Code \bullet V_{LSB}) + V_{OS}$$

V_{OUT} = The output voltage of the DAC measured at the given input code

DNL: Differential nonlinearity is the difference between the measured change and the ideal 1LSB change between any two adjacent codes. The DNL error between any two codes is calculated as below:

$$DNL = (\Delta V_{OUT} - V_{LSB})/V_{LSB}$$

ΔV_{OUT} = The measured voltage difference between two adjacent codes

The ΔV_{OUT} calculation includes the V_{OS} values to account for the effect of negative offset in Figure 1. This is relevant for code 1's DNL.

APPLICATIONS INFORMATION

OVERVIEW

The LTC1695 is a 5V brushless DC fan speed controller. Fan speed is controlled by linear regulating the applied voltage to the fan. To program fan speed, a system controller or microprocessor first sends a 6-bit digital code to the LTC1695 via a 2-wire SMBus/I^2C interface. The LTC1695's DAC then converts this digital code into a voltage reference. Finally, the LTC1695's op amp loop regulates the gate bias of the internal P-channel pass transistor to control the corresponding output voltage.

The LTC1695 is designed for portable, power-conscious systems that utilize small 5V brushless DC fans. These fans are increasingly popular in providing efficient cooling solutions in a small footprint. Smaller fans allow a user to employ multiple fans at strategic physical locations to govern a system's thermal airflow ("air duct" concept). These brushless DC fans also make use of the 5V supply used by the main digital/analog circuitry, removing the need for a 12V supply required by higher power fans.

The LTC1695's P-channel linear regulator control approach offers the lowest solution component count, the smallest PCB board space consumed, wide fan speed control range and low acoustical/electrical generated noise. Thermal concerns over the use of a linear regulator topology are eliminated by the fan's generally resistive behavior. As the LTC1695 DAC codes are changed to lower the output voltage, the voltage across the internal P-channel pass transistor increases. However, the fan's load current decreases almost linearly, thereby controlling power dissipation in the regulator. For example, a Micronel 5V, 0.7W fan ($40mm^2$ • 12mm) draws 80mA at 4V and 20mA at 2V. Thus the P-channel pass transistor's power loss decreases from 80mW to 60mW.

The LTC1695 incorporates several features to simplify the overall solution including a boost start timer to ensure fan start-up, output current limiting and thermal shutdown. The boost start timer is enabled via the SMBus commands and programs V_{OUT} to full scale for 250ms before regulating at the user programmed output voltage. This eliminates potential fan start-up problems at lower output voltage DAC codes.

The LTC1695's thermal shutdown circuit trips if die temperature exceeds 155°C. The P-channel pass transistor is shut off and bit D6 in the LTC1695's SMBus data register is set high. If an overload or short-circuit condition occurs, the LTC1695's current-limit circuitry limits output current to 390mA typically. In addition, bit D7 in the SMBus data register is set high. The readback capability of the LTC1695 allows the host controller to monitor the status of the D6 and D7 bits for fault conditions.

SMBus Serial Interface

The LTC1695 is an SMBus slave device that supports both SMBus send byte and receive byte protocol (Figure 2) with two interface signals, SCL and SDA.

The SMBus host initiates communication with the LTC1695 through a start bit followed by a 7-bit address code and a write bit. Each SMBus slave device in the system compares the address code with its specific address. For send byte and receive byte protocol, the write bit is LOW and HIGH respectively. If selected, the LTC1695 acknowledges by pulling SDA low.

If send byte protocol is used, the host issues an 8-bit command code. After receiving the entire command byte, the LTC1695 again acknowledges by pulling SDA low. At the falling edge of the acknowledge pulse, the LTC1695's DAC latches in the new command byte from its shift register.

If receive byte protocol is used, the LTC1695 acknowledges by pulling SDA low after the write bit. The LTC1695 then transmits the data byte. After the host receives the entire data byte, the cycle is terminated by a "NOT Acknowledge" bit and a stop bit.

APPLICATIONS INFORMATION

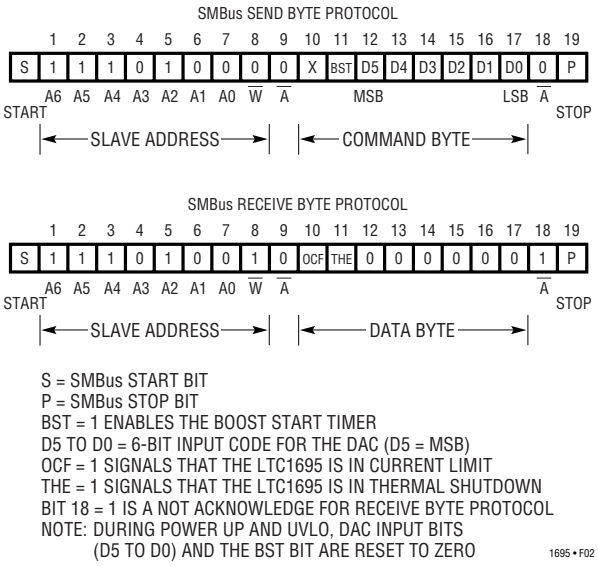


Figure 2. SMBus Interface Bit Definition

SCL and SDA

SCL is the synchronizing clock signal generated by the host. SDA is the bidirectional data transfer line between the host and a slave device. The host initiates a start bit by pulling SDA from high to low while SCL is high. The stop bit is initiated by changing SDA from low to high while SCL is high. All address, command and acknowledge signals must be valid and should not change while SCL is high. The acknowledge bit signals to the host the acceptance of a correct address byte or command byte.

The SCL and SDA input threshold voltages are typically 1.4V with 40mV of hysteresis. Connect the SCL and SDA open-drain lines to either a resistive or current source pull up. The LTC1695 SDA has an open-drain N-channel transistor capable of sinking 3mA at less than 0.4V during the slave acknowledge sequence.

The LTC1695 is compatible with the Philips/Signetics I^2C Bus Interface. The 1.4V threshold for SCL and SDA does not create any I^2C application problems.

Early Stop Conditions

If a stop condition occurs before the data byte is acknowledged in the write byte protocol, the LTC1695's DAC is not updated. Otherwise, the internal register is updated with the new data and V_{OUT} changes accordingly to the new programmed value.

Address, Command, Data Selection

The LTC1695's address is hard-wired internally as 1110100 (MSB to LSB, A6 to A0). Consult LTC for parts with alternate address codes. Consult the Address, Command and Data Byte Tables for further information and as a concise reference.

As shown in Figure 2, D5 to D0 in the command code, control the linear regulator's output voltage and thus fan speed. D5 to D0 are sent from the host to the LTC1695 during send byte protocol. The LTC1695 latches D5 to D0 as DAC input data at the falling edge of the data acknowledge signal. The host must set "BST" (boost start enable bit) to high if the LTC1695's 250ms boost start timer option is used. All bits are reset to zero during power-on reset and UVLO. As shown in the Timing Diagram, bit 6 and bit 7 in the data byte register are defined as thermal shutdown status (THE) and over current fault (OCF) status respectively. The LTC1695 sets OCF high if I_{LOAD} exceeds 390mA typically and "THE" high if junction temperature exceeds 155°C typically. The remaining bits of the data byte's register (bit 5 to 0) are set low during host read back.

APPLICATIONS INFORMATION

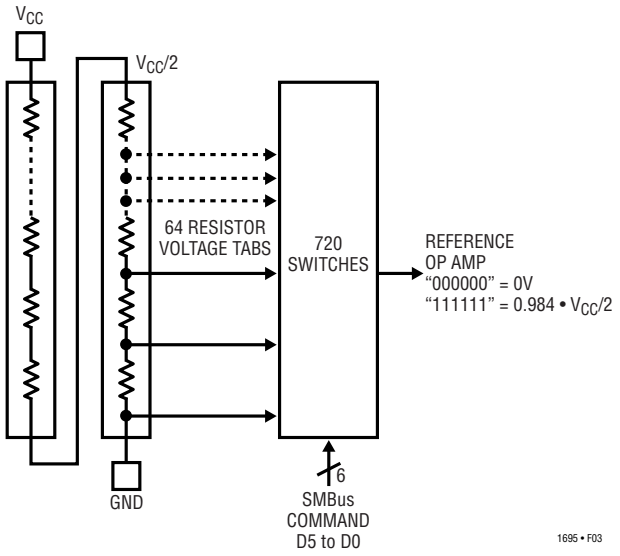


Figure 3. Ladder DAC

DAC

The LTC1695 uses a 128-segment resistor ladder to implement the monotonic 6-bit voltage DAC (Figure 3). Guaranteeing monotonicity (no missing codes) permits the use of the LTC1695 in thermal feedback control applications. As the typical application uses a 5V supply for V_{CC}, the reference for the 6-bit DAC is V_{CC}. LTC recommends a 10µF or greater tantalum capacitor to bypass V_{CC}. Users must account for the variation in the DAC's output absolute accuracy as V_{CC} varies. V_{CC} voltage should not exceed the absolute maximum rating of 7V or drop below the typical 2.8V undervoltage lockout threshold (UVLO) during normal operation.

The LTC1695's DAC specifications (INL, DNL, V_{OS}) account for the offset and gain errors of the linear regulator with respect to I_{LOAD}. Consult the Definitions section for more details.

The worst-case condition occurs if the LTC1695 P-channel pass transistor enters dropout at full-scale V_{OUT} and I_{LOAD}. Full-scale V_{OUT} (V_{FS}) is 4.922V with V_{CC} = 5V. In this condition, loop gain drops and gain error increases. The LTC1695 is designed for monotonicity up to V_{FS} with DNL and INL less than 0.75 LSB. Refer to the Electrical Characteristics and Typical Performance Characteristics for more information.

Linear Regulator Loop Compensation

The LTC1695's linear regulator approach is a simple and practical scheme for fan speed control featuring a wide and linear dynamic range. It also introduces less noise into the system supply rail, compared with a PWM scheme (fixed frequency, variable duty cycle), switching regulator topology or simple ON-OFF control.

The LTC1695 linear regulator feedback loop requires a capacitor at its output to stabilize the loop over the output voltage and load current range. The output capacitor value and the capacitor's ESR value are critical in stabilizing the LTC1695 feedback loop.

A ≥ 1µF general purpose, low to medium ESR (0.1Ω to 5Ω) tantalum or aluminium electrolytic capacitor is sufficient for most applications. These capacitor types offer a low-cost advantage, particularly for fan speed control applications. As the output capacitance value increases, stability improves. A typical 4.7µF, 1Ω ESR surface mount tantalum capacitor is recommended for the optimum transient response and frequency stability across temperature, V_{OUT} and I_{LOAD}. Refer to the load transient response waveforms in the Typical Performance Characteristics section.

The selection of the capacitor for C_{OUT} must be evaluated by the user for temperature variation of the capacitance and ESR value and the voltage coefficient of the capacitor value. For example, the ESR of aluminium electrolytic capacitors can increase dramatically at cold temperature. Therefore, the regulator may be stable at room temperature but oscillate at cold temperature. Ceramic capacitors with Z5U and Y5 dielectrics provide high capacitance values in a small package, but exhibit strong voltage and temperature coefficients (–80% in some cases). In addition, the ESR of surface mount ceramic capacitors is too low (<0.1Ω) to provide adequate phase-lead in the feedback loop for stability.

Fan Load and C_{LOAD}

Referring to Figure 4, C_{LOAD} varies greatly depending on the type of fan used. The simplest, inexpensive fans contain no protection circuitry and input capacitance is on the order of 200pF. More expensive fans generally incorporate a series-diode for reverse protection and input

APPLICATIONS INFORMATION

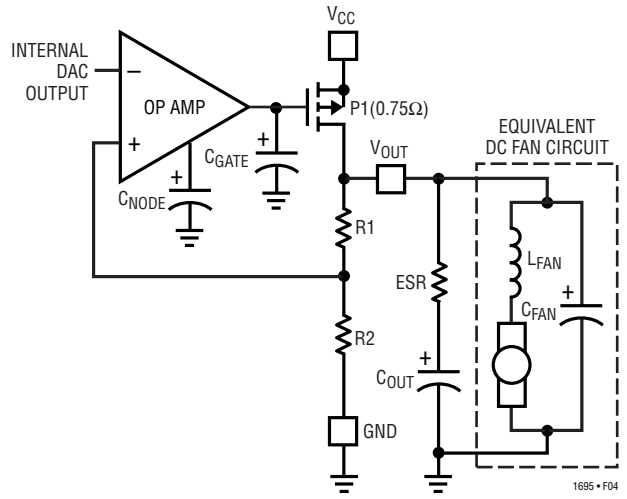


Figure 4. Regulator Feedback Loop

capacitance ranges from 2pF to 30pF. As previously discussed, an output bypass capacitor is required to stabilize the feedback loop. This output capacitor is in parallel with the fan's input capacitance and dominates the total capacitance. Thus, stability is generally not affected by the fan's input capacitance. The output capacitor also serves to filter the fan's output ripple during commutation of the fan's motor.

POR and UVLO

Under start-up conditions, the LTC1695 performs a power on reset (POR) function. The digital logic circuitry is disabled and the regulator is held off. The SMBus command register (to the DAC's input) and data register (current limit and thermal shutdown status) are reset to zero. The POR signal deactivates if V_{CC} rises above 2.9V typically. The LTC1695 is then allowed to communicate with the SMBus host and drive the fan accordingly. Upon exiting POR, the regulator's output voltage is set to V_{ZS} (code 0) until programmed by the SMBus host.

The LTC1695 enters UVLO if V_{CC} falls below 2.8V typically. Between 2.8V and 1V, the digital logic circuitry is disabled, the command/data registers are cleared and the regulator is shut down. In general, 100mV of hysteresis exists between the UVLO and POR thresholds.

Thermal Considerations

The LTC1695's power handling capability is limited by the maximum rated junction temperature of 125°C. Power dissipation (P_{DISS}) consists of two components:

1. Output current multiplied by the input/output voltage differential: $(I_{LOAD})(V_{CC} – V_{OUT})$, and
2. GND pin current multiplied by the input voltage: $(I_{GND})(V_{CC})$.

$$P_{DISS} = (I_{LOAD})(V_{CC} – V_{OUT}) + (I_{GND})(V_{CC})$$

$$T_J = P_{DISS} \bullet (\theta_{JA})$$

The LTC1695 has active current limiting and thermal shutdown circuitry for device protection during overload or fault condition. For continuous overload conditions, do not exceed the 125°C maximum junction temperature $T_{J(MAX)}$. Give careful consideration to all thermal resistance sources from junction to ambient. Consider any additional heat sources mounted in proximity to the LTC1695. This is particularly relevant in applications where the LTC1695's output is loaded with a constant I_{LOAD} and V_{OUT} is dynamically varied via the SMBus. At lower DAC output voltage codes, the increased input-to-output differential increases power dissipation if I_{LOAD} does not decrease.

For the LTC1695's 5-lead SOT-23 surface mount package, heat sinking is accomplished by using the heat spreading capabilities of the PC board and its copper traces (in particular, the GND pin trace).

The following table lists measured thermal resistance results for various size boards and copper areas. All measurements were taken in still air on 3/32" FR-4 board with one ounce copper.

Table 2. Measured Thermal Resistance (θ_{JA})

Copper Area		Board Area	Thermal Resistance (Junction to Ambient)
Topside*	Backside		
2500mm^2	2500mm^2	2500mm^2	125°C/W
1000mm^2	2500mm^2	2500mm^2	125°C/W
225mm^2	2500mm^2	2500mm^2	130°C/W
100mm^2	2500mm^2	2500mm^2	135°C/W
50mm^2	2500mm^2	2500mm^2	150°C/W

*Device is mounted on topside

APPLICATIONS INFORMATION

For further information, refer to the Junction Temperature Increase (above ambient temperature) vs I_{LOAD} graph in the Typical Performance Characteristics section. This graph provides a fast and simple junction temperature estimation with various V_{OUT} (DAC code) and I_{LOAD} combinations for a typical application.

Boost Start Timer

In general, a 5V brushless DC fan starts at a voltage value higher than the voltage at which it stalls. This behavior is directly attributed to the force necessary to overcome the back EMF of the fan. For example, one fan measured started at 3.5V but operated until its terminal voltage fell below 2.1V. Therefore, users must ensure start-up in the fan before programming the fan voltage to a value lower than the starting voltage. Monitoring the fan's DC current for a stalled condition does not work due to the fan's resistive nature. Fans can sink load current even though they are not rotating. Other approaches include detecting absence of the fan's commutation ripple current and tachometers. In general, these approaches are more complex, require more circuitry, add cost and have to be customized for the specific fan used.

The LTC1695 contains a programmable boost start timer offering three flexible solutions to the user:

1.) Enable the boost start timer bit (D6 in the DAC command code). Each time a new output voltage is programmed, the timer forces V_{OUT} to full scale (4.922V nominal with V_{CC} = 5V) for 250ms before assuming the programmed output voltage value. This ensures fan start up even if the programmed output voltage is below the fan's start threshold.

2.) Users may also choose to use a software timer routine inside the host controller to power the DC fan, at full scale, for a programmed time period before programming V_{OUT} to a lower desired DAC output voltage code.

3.) Users may choose a tachometer fan that feedbacks its speed to the SMBus host. If fan stall conditions are detected, the SMBus host re-programs the LTC1695.

Beyond a typical 125°C LTC1695 junction temperature, the boost start timer (if activated) maintains V_{OUT} at full scale (V_{FS}) until junction temperature decreases to approximately 105°C. This extended timer period is an attempt to cool down the system and the LTC1695 by running the fan at full speed. In most cases, such elevated ambient temperatures require the fan to run at full speed anyway. The remaining LTC1695's functionality remains unchanged.

Thermal Shutdown, Overcurrent

The LTC1695 shuts down the P-channel linear regulator if die temperature exceeds 155°C typically. The thermal shutdown circuitry employs about 30°C of hysteresis. As previously mentioned, the LTC1695 sets bit 6 (THE) in the SMBus data byte register HIGH during thermal shutdown conditions. During a fault condition, the LTC1695's SMBus logic continues to operate so that the SMBus host can read back the fault status data.

During an overload or short-circuit fault condition, the LTC1695's current-limit detector sets bit 7 (OCF) in the SMBus data byte register HIGH and actively limits output current to 390mA typically. This protects the LTC1695's P-channel pass transistor. Under dead short conditions with V_{OUT} = 0V, the LTC1695 also clamps the output current. However, the increased power dissipation (5V • 390mA = 1.95W) eventually forces the LTC1695 into thermal shutdown. The LTC1695 will then thermally oscillate until the fault condition is removed.

During recovery from thermal shutdown (typically 125°C), the LTC1695 automatically activates the boost start timer, programming the fan voltage to full scale for 250ms (T_{BST_ST}), before switching to the user programmed output voltage value. This again eliminates fan start-up problems if the thermal shutdown fault occurred while the fan was previously operating at an output voltage below the fan's starting voltage. In addition, as discussed, the boost start timer will keep V_{OUT} at V_{FS} for an extended time period beyond T_{BST_ST} until the LTC1695's junction temperature drops below 105°C.

The LTC1695's protection features protect itself, the fan, and more importantly alerts the SMBus host to any system thermal management fault conditions.

APPLICATIONS INFORMATION

DC FAN SELECTION

The LTC1695, in the 5-lead SOT-23 package, caters mainly to 5V brushless DC fans, in spot cooling and notebook computer applications, that consume less than 1W maximum. These applications typically require fan footprints on the order of 4000mm^3 to 20000mm^3. Such fan sizes are common and commercially available. Examples of these miniature fans are the "Ultra-thin DC fan" and "Extra-mini DC fan" from SUNON Inc. Models in these series range from 17mm to 40mm in size, weigh from 4 grams to 10 grams and provides airflow densities from 0.65 CFM to 6 CFM.

Users must consider parameters like physical size (L • W • H), airflow (CFM), power dissipation (W) and acoustically generated noise (dBA) when choosing a fan. Users must also evaluate the fan's I-V characteristics versus fan speed and the start/stall characteristics of the fan. Other factors include mechanical considerations such as low cost sleeve bearings or ball bearings that have better long term reliability. Finally, users must consider if the fan requires any input protection features such as reverse-voltage protection. All of these factors affect the fan's cost.

Table 3 lists some 5V fan manufacturer's contact information.

Table 3. 5V DC Fan Manufacturers

Manufacturer	Address
SUNON Inc.	1075 W. Lambert Rd., Brea, CA 92821 Tel: (714)255-0208 Website: http://www.sunon.com
Advanced Technology Company	1280 Liberty Way, Vista, CA 92083 Tel: (760)727-7430
Nidec America	152 Will Dr., Canton, MA 02021 Tel: (781)828-6216 Website: http://nidec.com
NMB Technologies Inc.	9730 Independence Ave., Chatsworth, CA 91311 Tel: (818)341-3355 Website: http://www.nmbtech.com
Micronel	1280 Liberty Way, Vista, CA 92083 Tel: (760)727-7400 Website: http://www.micronel.com

Table 4 lists some 5V brushless DC fans suitable for typical LTC1695 fan speed control applications. Figure 5 shows the measured I-V characteristics of these fans. For a particular fan selection, users must determine the minimum DAC output voltage code below which the fan stalls. Most fans continue to consume current, even in a stalled condition.

Table 4. Some 5V DC Fans' Characteristics

Manufacturer	Part Number	Airflow (CFM)	Power (W)	Size (L • W • H)mm^3
SUNON	KDE0501PFB2-8	0.65	0.50	20 • 20 • 10
ATC	AD0205HB-G51	0.80	0.45	25 • 25 • 10
SUNON	KDE0502PFB2-8	1.70	0.60	25 • 25 • 10
SUNON	KDE0503PFB2-8	3.20	0.60	30 • 30 • 10
SUNON	KDE0535PFB2-8	4.80	0.70	35 • 35 • 10
Micronel	F41MM-005XK-9	6.10	0.70	40 • 40 • 12

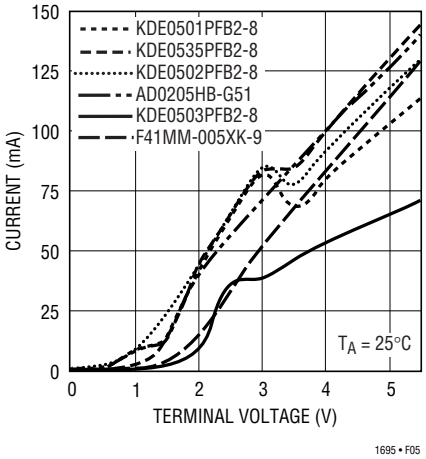


Figure 5. I-V Characteristics of 5V Brushless DC Fan Samples

APPLICATIONS INFORMATION

SMBus Address Byte Table

Decimal	HEX	SMBus Protocol
232	E8	Send Byte to the LTC1695
233	E9	Receive Byte from the LTC1695

The LSB of the SMBus address is the write bit. For send byte protocol, $\overline{W} = 0$. For Receive byte protocol, $\overline{W} = 1$

SMBus Command Byte Table (Send Byte Protocol)

DECIMAL (D5 to D0)	BINARY MSB LSB	HEX (D6-D7 set to 0)	Nominal V_{OUT}(V) I_{LOAD} = 1mA
0	X0000000	00	0.000
1	X0000001	01	0.078
2	X0000010	02	0.156
3	X0000011	03	0.234
4	X0000100	04	0.313
5	X0000101	05	0.391
6	X0000110	06	0.469
7	X0000111	07	0.547
8	X0001000	08	0.625
9	X0001001	09	0.703
10	X0001010	0A	0.781
11	X0001011	0B	0.859
12	X0001100	0C	0.938
13	X0001101	0D	1.016
14	X0001110	0E	1.094
15	X0001111	0F	1.172
16	X0010000	10	1.250
17	X0010001	11	1.328
18	X0010010	12	1.406
19	X0010011	13	1.484
20	X0010100	14	1.563
21	X0010101	15	1.641
22	X0010110	16	1.719
23	X0010111	17	1.797
24	X0011000	18	1.875
25	X0011001	19	1.953
26	X0011010	1A	2.031
27	X0011011	1B	2.109
28	X0011100	1C	2.188
29	X0011101	1D	2.266
30	X0011110	1E	2.344
31	X0011111	1F	2.422

D6 = 0 disables the boost start timer.
D7 = X = don't care

SMBus Data Byte Table (Receive Byte Protocol)

DECIMAL	BINARY MSB LSB	HEX	LTC1695 Status
0	00000000	00	No Fault
128	10000000	80	Overcurrent Fault/Clamp
64	01000000	40	Thermal Shutdown

During thermal shutdown, the LTC1695's LDO is shut off.

DECIMAL (D5 to D0)	BINARY MSB LSB	HEX (D6-D7 set to 0)	Nominal V_{OUT}(V) I_{LOAD} = 1mA
32	X0100000	20	2.500
33	X0100001	21	2.578
34	X0100010	22	2.656
35	X0100011	23	2.734
36	X0100100	24	2.813
37	X0100101	25	2.891
38	X0100110	26	2.969
39	X0100111	27	3.047
40	X0101000	28	3.125
41	X0101001	29	3.203
42	X0101010	2A	3.281
43	X0101011	2B	3.359
44	X0101100	2C	3.438
45	X0101101	2D	3.516
46	X0101110	2E	3.594
47	X0101111	2F	3.672
48	X0110000	30	3.750
49	X0110001	31	3.828
50	X0110010	32	3.906
51	X0110011	33	3.984
52	X0110100	34	4.063
53	X0110101	35	4.141
54	X0110110	36	4.219
55	X0110111	37	4.297
56	X0111000	38	4.375
57	X0111001	39	4.453
58	X0111010	3A	4.531
59	X0111011	3B	4.609
60	X0111100	3C	4.688
61	X0111101	3D	4.766
62	X0111110	3E	4.844
63	X0111111	3F	4.922

D6 = 0 disables the boost start timer.
D7 = X = don't care

APPLICATIONS INFORMATION

SMBus Command Byte Table (Boost Start Timer Enabled)

DECIMAL (D5 to D0)	BINARY MSB LSB	HEX (D7 set to 0)	Nominal V_{OUT}(V) I_{LOAD} = 1mA
0	X1000000	40	0.000
1	X1000001	41	0.078
2	X1000010	42	0.156
3	X1000011	43	0.234
4	X1000100	44	0.313
5	X1000101	45	0.391
6	X1000110	46	0.469
7	X1000111	47	0.547
8	X1001000	48	0.625
9	X1001001	49	0.703
10	X1001010	4A	0.781
11	X1001011	4B	0.859
12	X1001100	4C	0.938
13	X1001101	4D	1.016
14	X1001110	4E	1.094
15	X1001111	4F	1.172
16	X1010000	50	1.250
17	X1010001	51	1.328
18	X1010010	52	1.406
19	X1010011	53	1.484
20	X1010100	54	1.563
21	X1010101	55	1.641
22	X1010110	56	1.719
23	X1010111	57	1.797
24	X1011000	58	1.875
25	X1011001	59	1.953
26	X1011010	5A	2.031
27	X1011011	5B	2.109
28	X1011100	5C	2.188
29	X1011101	5D	2.266
30	X1011110	5E	2.344
31	X1011111	5F	2.422
32	X1100000	60	2.500
33	X1100001	61	2.578
34	X1100010	62	2.656
35	X1100011	63	2.734
36	X1100100	64	2.813
37	X1100101	65	2.891
38	X1100110	66	2.969
39	X1100111	67	3.047
40	X1101000	68	3.125
41	X1101001	69	3.203
42	X1101010	6A	3.281
43	X1101011	6B	3.359
44	X1101100	6C	3.438
45	X1101101	6D	3.516
46	X1101110	6E	3.594
47	X1101111	6F	3.672
48	X1110000	70	3.750
49	X1110001	71	3.828
50	X1110010	72	3.906
51	X1110011	73	3.984
52	X1110100	74	4.063
53	X1110101	75	4.141
54	X1110110	76	4.219
55	X1110111	77	4.297
56	X1111000	78	4.375
57	X1111001	79	4.453
58	X1111010	7A	4.531
59	X1111011	7B	4.609
60	X1111100	7C	4.688
61	X1111101	7D	4.766
62	X1111110	7E	4.844
63	X1111111	7F	4.922

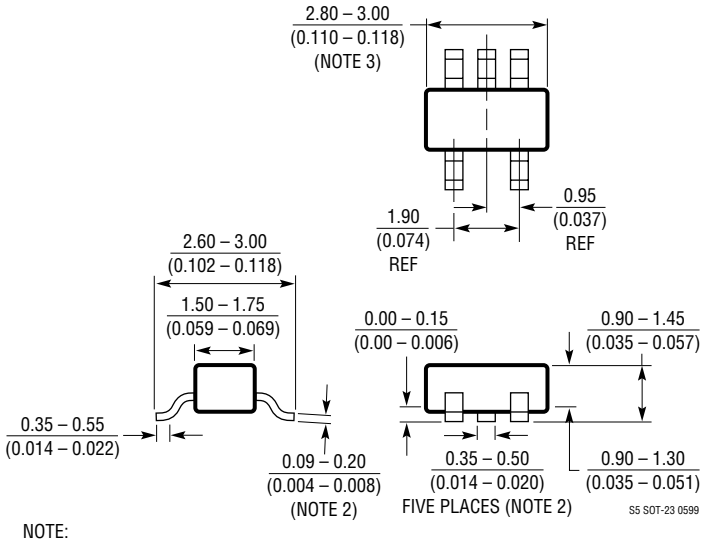
D6 = 1 enables the boost start timer.
D7 = X = don't care

D6 = 1 enables the boost start timer.
D7 = X = don't care

PACKAGE DESCRIPTION

Dimensions in inches (millimeters) unless otherwise noted.

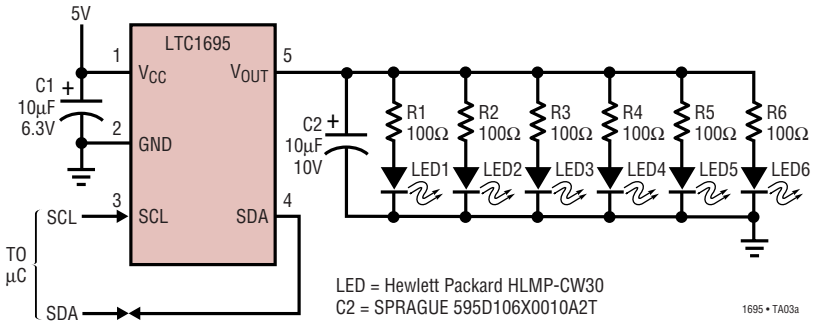
S5 Package
5-Lead Plastic SOT-23
(LTC DWG # 05-08-1633)



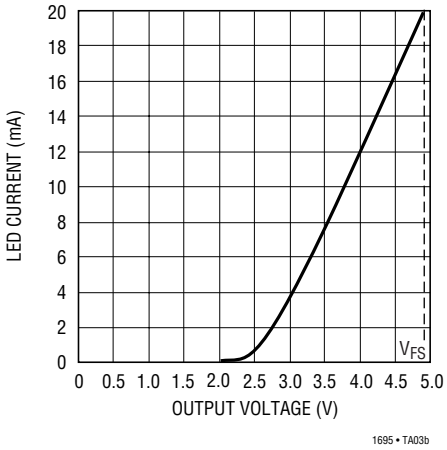
NOTE:
1. DIMENSIONS ARE IN MILLIMETERS
2. DIMENSIONS ARE INCLUSIVE OF PLATING
3. DIMENSIONS ARE EXCLUSIVE OF MOLD FLASH AND METAL BURR
4. MOLD FLASH SHALL NOT EXCEED 0.254mm
5. PACKAGE EIAJ REFERENCE IS SC-74A (EIAJ)

TYPICAL APPLICATION

SMBus I²C Controlled White LED Driver



Output Voltage vs LED Current



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT1120	125mA Low Dropout PNP Linear Regulator with 40µA Quiescent Current	0.6V Dropout Voltage at 125mA
LT1121	150mA Low Dropout PNP Linear Regulator with 30µA Quiescent Current	0.5V Dropout Voltage at 150mA, SO8/SOT-223 package
LTC1380/LTC1393	Single-Ended 8-Channel/Differential 4-Channel Analog Mux with SMBus Interface	Low R_{ON}: 35Ω Single-Ended/70Ω Differential, Expandable to 32 Single or 16 Differential Channels
LTC1427-50	Micropower, 10-Bit Current Output DAC with SMBus Interface	Precision 50µA ± 2.5% Tolerance Over Temperature, 4 Selectable SMBus Addresses, DAC Powers up at Zero or Midscale
LT1521	300mA Low Dropout PNP Linear Regulator with 12µA Quiescent Current	0.5V Dropout Voltage at 150mA, SO8/SOT-223 Package
LTC1623	Dual High Side Switch Controller with SMBus Interface	8 Selectable Addresses/16-Channel Capability
LTC1663	SMBus Interface 10-Bit Rail-to-Rail Micropower DAC	DNL < 0.75LBS Max, 5-Lead SOT-23 Package
LTC1694/LTC1694-1	SMBus Accelerator	Improved SMBus/I²C Rise Time, Ensures Data Integrity with Multiple SMBus/I²C Devices
LT1761	100mA, Low Noise, LDO Micropower Regulator	0.3V Dropout Voltage at 100mA, SOT-23 Package
LT1762	150mA, Low Noise, LDO Micropower Regulator	0.3V Dropout Voltage at 150mA, MSOP Package
LT1786F	SMBus Controlled CCFL Switching Regulator	1.25A, 200kHz, Floating or Grounded Lamp Configurations

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